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*Research Article*

# A New Synchronization Technique of a Three-Phase Grid Tied Inverter for Photovoltaic Applications

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Three-phase grid synchronization is one of the main techniques of the three-phase grid connected power inverters used in photovoltaic systems. This technique was used to reach the fast and accurate three-phase grid tied inverter synchronization. In this paper a new synchronization method is presented on the basis of integrating the grid voltage two times (line-to-line or phase voltage). This method can be called "double integral synchronization method" (DISM) as it integrates the grid voltage signals two times to generate the reference signals of three-phase photovoltaic inverter currents. DISM is designed and simulated in this paper to operate in both analog and digital circuits of three-phase photovoltaic inverter system with the same topology. The digital circuit design and dsPIC33FJ256GP710A as a microcontroller (the dsPIC33FJ256GP710A with the Explorer 16 Development Board from microchip) was used practically in this paper to generate and control the sine pulse width modulation (SPWM) technique according to DISM for three-phase photovoltaic inverter system. The main advantage for this method (DISM) is learning how to eliminate the integration constant to generate the reference signals without needing any reference signals or truth table, just the line-to-line or phase voltage of grid.

## 1. Introduction

Due to the continuous rise in energy consumption, the demand for electricity and its efficiency has increased in the world. Some countries have tended to adopt small renewable energy sources linked to power transmission lines with traditional energy sources. Solar energy is one of the most important sources of renewable energy in the world today.

The synchronization is the first item of any closed control system of single or three-phase inverter connected to grid [1]. The purpose of a synchronization method is to generate the reference signal for a pulse width modulation (PWM). There are many synchronization methods to synchronize to the reference signal of three-phase inverter connected to grid [2–5], like PLL using a local oscillator comparison and sine wave tables [6, 7].

This paper focuses on using a new synchronization method to set up the three-phase reference signals of measuring current depending on line-to line or phase voltage of grid without a phase or frequency generation. This method is called double integral synchronization method (DISM).

The double integration method in power electronic or power system is a procedure to set the references value (voltage or current ) in the time[8, 9]. Equation (1) describes the double integration of the grid voltage.

$$I_{Ref} = \iint V_{(t)} dt^2, \tag{1}$$

where $V_{(t)}$ is the line-to-line voltage or phase voltage of grid.

Double integration is also used in other applications where a solution is needed to avoid a DC integrating constant. Figure 1 shows the block diagram of double integral method depending on (1). Double integral synchronization circuit in this paper can be divided into two types.

(1) Analog circuit design of DISM.

(2) Digital circuit design of DISM.

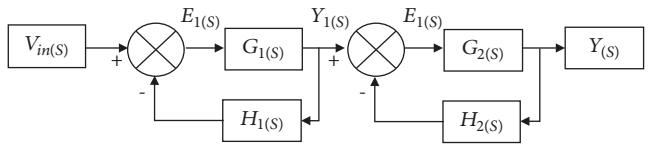


Figure 1: The double integral method block diagram (DISM).

The analog circuit is designed for single and three-phase double integral synchronization method. The integration circuits designed and simulated are identical for the first and second integration for single phase. All the signals and equations for three-phase inverter were derived based on Figure 1. The digital circuit of DSIM is designed and simulated according to the same parameters and equations of analog circuit. Then, the digital circuits of DISM are implemented on hardware by using the dsPIC33FJ256GP710A with the Explorer 16 Development Board from microchip to generate the PWM of three-phase inverter. The dsPIC33FJ256GP710A is a one type of 16-bit microcontroller which has been used due to this type of microcontroller being used in industrial application [10–13]. The sine pulse width modulation (SPWM) technique is used for three-phase photovoltaic inverter system [14, 15]. Analog and digital models and simulation circuits in this paper were performed by using MATLAB/Simulink software program.

The aim of this work is to design, simulate, and implement new analog and digital circuit to synchronize the generated current from three-phase photovoltaic inverter system with grid without needing any reference signals or truth table (just the line-to-line or phase voltage of grid).

The rest of the paper is organised as follows: Section 2 presents the related work review, Section 3 presents the mathematic model of DISM, Section 4 discusses the simulation design and results of (DISM), Section 5 discusses the experimental setup of SPWM for Three-Phase DISM, and, finally, Section 6 shows conclusions and further work.

$V_{in(S)}$ is the input signal, $Y_{1(S)}$ is the output of the first integral, and $Y_{(S)}$ is the output (double integral) signal.

## 2. Related Work Review

The famous synchronization method of output reference signals in electronic and power application is a Phase Locked Loop. The Phase Lock Loop (PLL) is a control system designed to generate the reference output signals related to the input signals for each phase. There are different types of PLL methods in the world of electronic and communication system [1–7, 16–26]. These PLL control systems are designed according to variable frequency and signal phase detector in feedback signals loop, PLL filtering technique, and PLL prefiltering technique.

Table 1 presents the most famous six PLL in power electronic application according to the simplicity of design, adaptivity of frequency, distortion for insensitivity, and balance sensitivity.

## 3. Mathematic Model of Double Integration Synchronization Method

The integration in mathematics means finding area under the curve or finding the volume of solids for double integral. In a steady state sine wave a double integration corresponds to 180o phase rotation is an inverted signal. So, it can be used as a way to synchronize voltage and current of the grid. The art will be to be able to remove the DC component without introducing a phase shift. The double integration is used in synchronization method of three-phase inverter signals. The double integration method in power electronic or power system is a procedure to set the references value (voltage or current) for slope and deflection at points along the time axis. The double integration block diagram in Figure 1 is one in which the output signal is directly proportional to the change of the input signal with respect to time without needing any external or reference signal to compare with output signal. The transfer function of double integral method in Figure 1 is given in (2). According to Figure 1 and (2), the description for this system is specified in (3)-(5).

$$\frac{\mathrm{Y}(\mathrm{S})}{\mathrm{V_{in}}(\mathrm{s})} = \frac{Y(s)}{Y_1(s)} * \frac{Y_1(s)}{V_{in}(s)} \tag{2}$$

| **First Integral** | **Second Integral** |
|---|---|
| $Y_1(s) = E_1(s) * G_1(s)$ | $Y(s) = E_2(s) * G_2(s)$ |
| $E_1(S) = V_{in}(s) - Y_1(S) * H_1(S)$ | $E_2(S) = Y_1(s) - Y(S) * H_2(S)$ |
| $V_{in}(s) = E_1(s)\left(1 + G_1(s) * H_1(s)\right)$ | $Y_1(s) = E_2(s)\left(1 + G_2(s) * H_2(s)\right)$ |

(3)

$$\frac{Y_1(s)}{V_{in}(s)} = \frac{G_1(s)}{1 + G_1(s)H_1(s)} \qquad \frac{Y(s)}{Y_1(s)} = \frac{G_2(s)}{1 + G_2(s)H_2(s)} \tag{4}$$

$$\frac{Y(s)}{V_{in}(s)} = \frac{G_1(s)}{1 + G_1(s) * H_1(s)} * \frac{G_2(s)}{1 + G_2(s) * H_2(s)} = \left(\frac{G(s)}{1 + G(s) * H(s)}\right)^2 \tag{5}$$

Table 1: List of related work review.

| Related Work Reference | Type of PLL | The Simplicity of Design | Adaptive of Frequency | Distortion for Insensitivity | Balance Sensitivity |
|---|---|---|---|---|---|
| Masoud Karimi-Ghartemani and M. Reza Iravani[23], 2004 | EPLL | ★★ | ★★ | ★★★ | ★★★ |
| Houshang Karimi et al[21], 2004 | QPLL | ★★ | ★★ | ★★★ | --- |
| Shinji Shinnaka[20], 2008 | RPLL | ★★ | ★★ | ★★★ | --- |
| Kyoung-Jun Lee et al[25], 2014 | APLL | ★★ | ★★ | ★★★ | ★★★ |
| H. Shokrollah Timorabadi and F. P. Dawson[22], 2007 | PPLL | ★★ | ★★★ | ★★★ | ★★★ |
| Sidelmo M. Silva[24], 2004 | SFPLL | ★★★ | ★★ | ★★ | ★ |

**★★★: good, ★★: average, and ★: poor.**
**EPLL:** Enhanced Phase Locked Loop; **APLL:** Adaptive Phase Locked Loop.
**QPLL:** Quadrature Phase Locked Loop; **PPLL:** Predictive Phase Locked Loop.
**RPLL:** Robust Single Phase Locked Loop; **SF-PLL:** Synchronous Frame Phase Locked Loop.

The single phase circuit of DISM in Figure 2(a) consists of two integral circuits with the same parameters to set up the reference value for current or voltage. According the (2)-(5), the output signal transfer function of the first stage (first integral) is given as in

$$V_{A1} = \left(\frac{1}{R_{11}C_{11}S}\right)V_{ph1} - \left(\frac{1 + R_{11}C_{11}S}{R_{11}C_{11}S}\right)V_{SA1}, \quad (6)$$

where $V_{SA1}$ is the feedback of the first signal (DC offset signal of integral) and it is defined in

$$V_{SA1} = \left(\frac{R_{12}C_{12}S + 1}{R_{13}C_{12}S}\right)\left(\frac{R_{15}}{R_{14} + R_{15}}\right)\left(\frac{1}{R_{16}C_{13}S + 1}\right)V_{A1} \quad (7)$$

In an analog circuit design ($R_{12} * C_{12} = R_{16} * C_{13}$ and $R_{22} * C_{22} = R_{26} * C_{23}$) then, the final feedback signal is presented in (7):

$$V_{SA1} = \left(\frac{1}{R_{13}C_{12}S}\right)\left(\frac{R_{15}}{R_{14} + R_{15}}\right)V_{A1} \quad (8)$$

Equations (9) and (10) are transfer function of the second stage (second integral) represented as the same equations above ((6) and (8)).

$$V_{A2} = \left(\frac{1}{R_{21}C_{21}S}\right)V_{A1} - \left(\frac{1 + R_{21}C_{21}S}{R_{21}C_{21}S}\right)V_{SA2} \quad (9)$$

$$V_{SA2} = \left(\frac{1}{R_{23}C_{22}S}\right)\left(\frac{R_{25}}{R_{24} + R_{25}}\right)V_{A2} \quad (10)$$

The output signal of the second integral has a phase shift (**180°**). Then, the inverse of the double integral is matched with the input signal.

$$V_A = -V_{A2} \quad (11)$$

The reference signal of the three phase signals (voltage or current) is presented in (12)-(14) depending on Figure 2(b) and (6)-(11):

$$\begin{bmatrix} V_{A1} \\ V_{B1} \\ V_{C1} \end{bmatrix} = [A_1 - B_1]\begin{bmatrix} V_{ph1} & V_{ph2} & V_{ph3} \\ V_{SA1} & V_{SB1} & V_{SC1} \end{bmatrix}; \quad (12)$$

$$\begin{bmatrix} V_{A2} \\ V_{B2} \\ V_{C2} \end{bmatrix} = [A_2 - B_2]\begin{bmatrix} V_{A1} & V_{B1} & V_{C1} \\ V_{SA2} & V_{SB2} & V_{SC2} \end{bmatrix}$$

$$\begin{bmatrix} V_{SA1} \\ V_{SB1} \\ V_{SC1} \end{bmatrix} = D_1.\begin{bmatrix} V_{A1} \\ V_{B1} \\ V_{C1} \end{bmatrix}; \quad (13)$$

$$\begin{bmatrix} V_{SA2} \\ V_{SB2} \\ V_{SC2} \end{bmatrix} = D_2.\begin{bmatrix} V_{A2} \\ V_{B2} \\ V_{C2} \end{bmatrix}$$

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = -\begin{bmatrix} V_{A2} \\ V_{B2} \\ V_{C2} \end{bmatrix}, \quad (14)$$

where

$$A_1 = A_2 = \left(\frac{1}{R_{11}C_{11}S}\right);$$

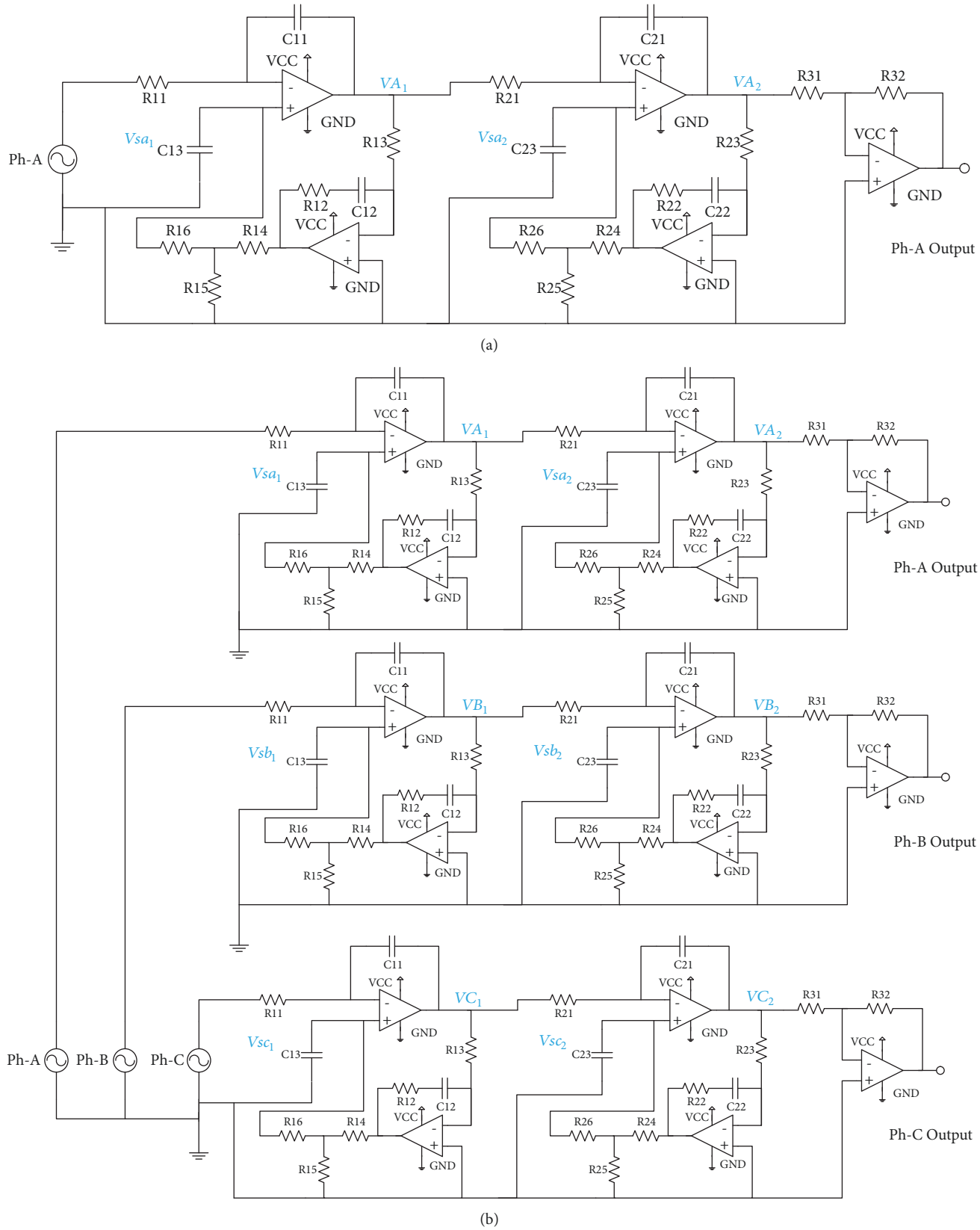


Figure 2: The analog circuit of DISM (a) single phase circuit; (b) three-phase circuit.

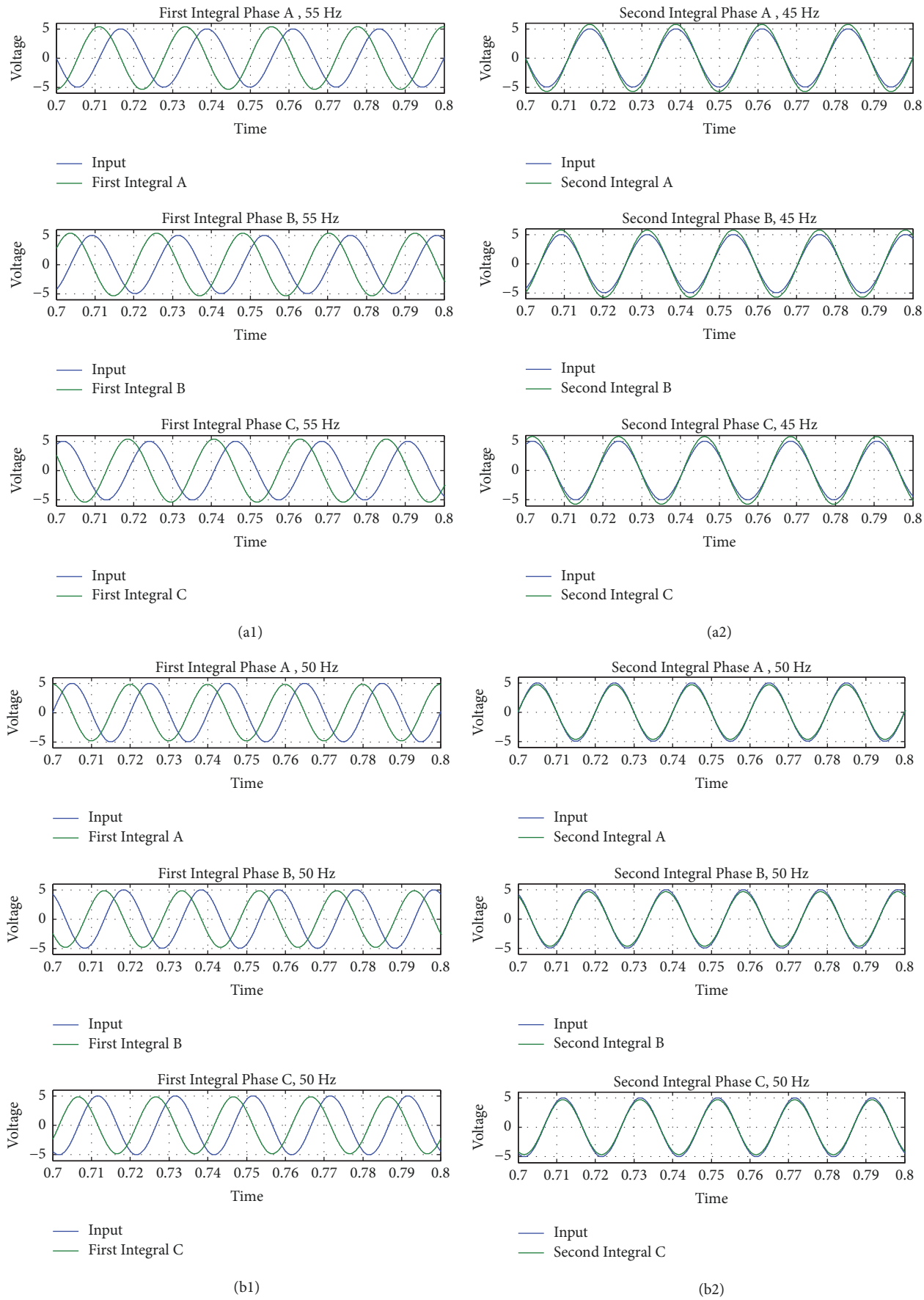


Figure 3: Continued.

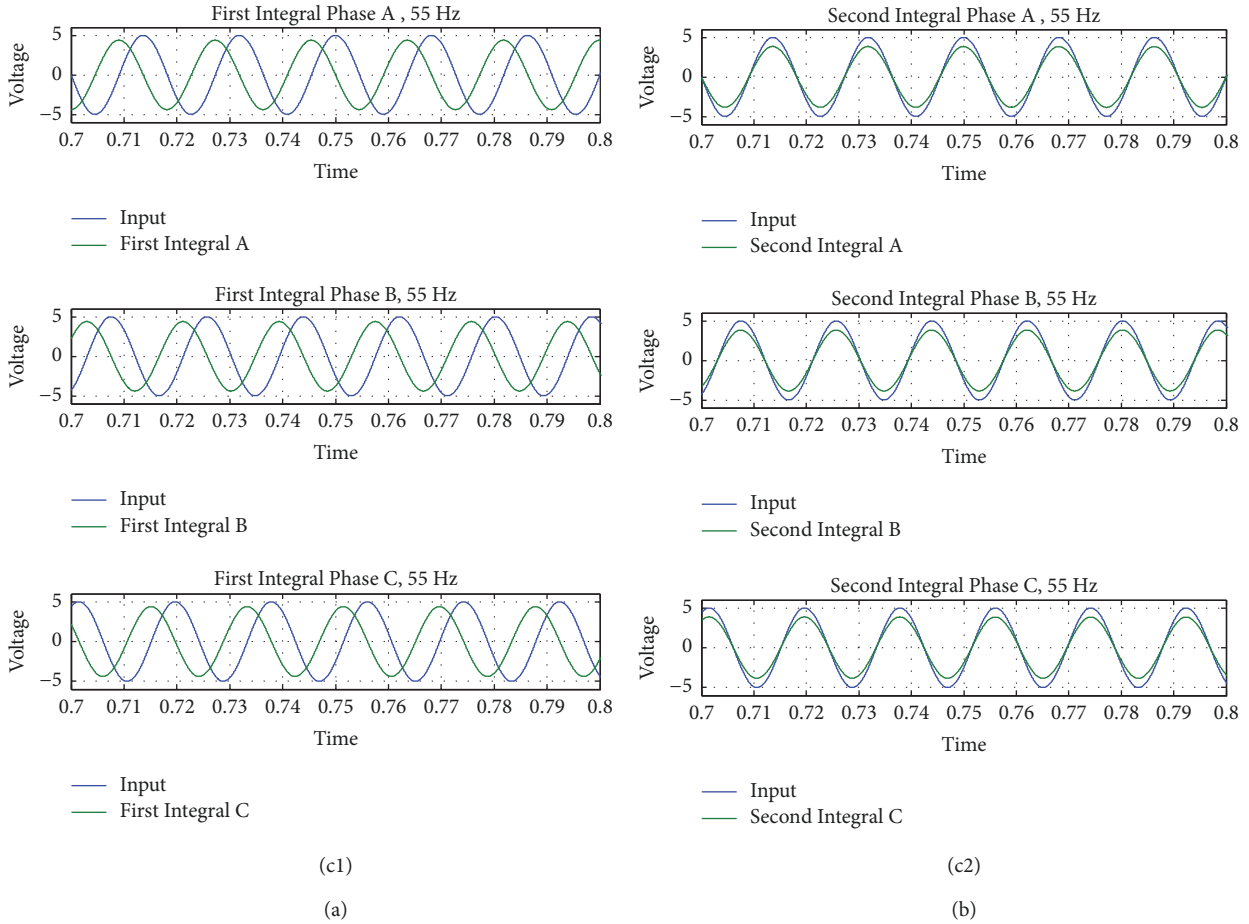


FIGURE 3: Analog simulation result (45, 50, and 55) Hz: (a) three-phase output signals (first integral); (b) three-phase output signals (inverse of double integral).

$$B_1 = B_2 = \left(\frac{1 + R_{11}C_{11}S}{R_{11}C_{11}S}\right);$$
$$D_1 = D_2 = \left(\frac{1}{R_{13}C_{12}S}\right)\left(\frac{R_{15}}{R_{14} + R_{15}}\right) \quad (15)$$

VA1, VB1, and VC1 are three-phase output signal of first stage and VA, VB, and VC are three-phase output reference signals.

## 4. Simulation Results of DISM

Double integration synchronization circuit diagram in Figure 1 can be divided into two categories.

*4.1. Analog Circuit Simulation (Analysis and Result).* According to (11), (12), and (13) and the three-phase analog circuit in Figure 2(b), the simulation signals' result for three-phase system was presented in Figure 3, with three deferent values of input signals frequency (45,50, and 50 Hz).

Figures 3 (a1), (b1), and (c1) present the simulation results of the first integral. These figures present the output signals of three phases according to the input voltage with frequencies 45, 50, and 55 Hz, respectively. The phase shift between the input and output signal of the first integral is ($90^0$).

Figures 3 (a2), (b2), and (c2) present the simulation results of the inverse of the double integral method following the second integration of the phase shift between the output and input signal which is ($180^o$). Then, the inverse of the double integral is shown in Figure 3(b). The phase shift between the final output and input signals for the three-phase analog circuit in Figure 3 is 0 seconds for 50Hz, 75 $\mu$ seconds lagging for 45Hz, and 50 $\mu$ seconds leading for 55Hz.

*4.2. Digital Circuit Simulation (Analysis and Result).* The digital circuit block diagram of DISM in Figure 4 was designed according to the design of the block diagram in Figure 1 and the analog circuit in Figure 2(a) (single and three-phase DISM) and (5)-(14).

Figure 5 shows the three-phase simulation results of the digital circuit of DISM (input, first integral, and the output) signals. Figures 5(a1), (a2) and (a3) show the results independent of line-to-line sin wave voltage and frequencies (45, 50, and 55) Hz, respectively. Figures 5 (b1), (b2), and (b3) show the results independent of square wave voltage and same frequencies above. The result of sine wave and

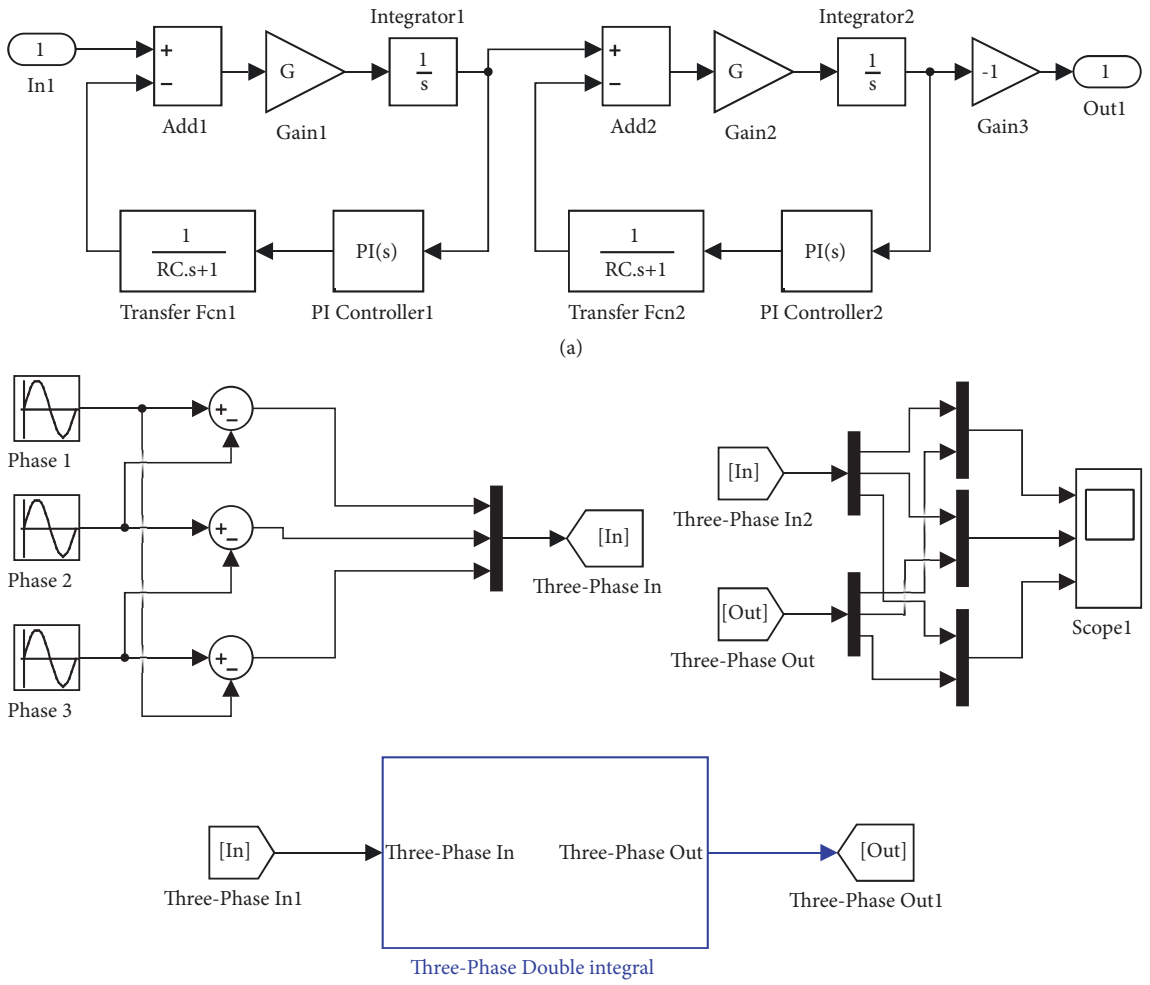


Figure 4: The digital block diagram of DISM: (a) single phase; (b) three-phase.

Table 2: Phase shift delay between input and output.

| The Frequency (Hz) | Phase Shift ($\mu$S) | Status |
|---|---|---|
| 35 | 400 | lagging |
| 40 | 200 | lagging |
| 45 | 75 | lagging |
| 50 | 0 | === |
| 55 | 50 | leading |
| 60 | 75 | leading |
| 65 | 100 | leading |
| 70 | 100 | leading |

square wave was approved by the DISM. The system designed depending on 50Hz as reference value. Then, the phase shift between input and output signals is equal to zero for 50 Hz. When the frequency increases greater than 50Hz, the phase shift between input and output signals is leading and if the frequency decreases less than 50Hz, the phase shift is lagging. The phase shift values between input and output signals of digital circuit DISM was presented in Table 2, depending on frequencies from 35Hz to 70Hz.

The single phase bode blot diagram for the first and second stage of DISM in Figure 4(a) is shown in Figure 6. Figure 6 presents the result for three frequencies (45, 50, and 55) Hz. It can be seen that the three-phase signal shows good performance of designed DISM controller.

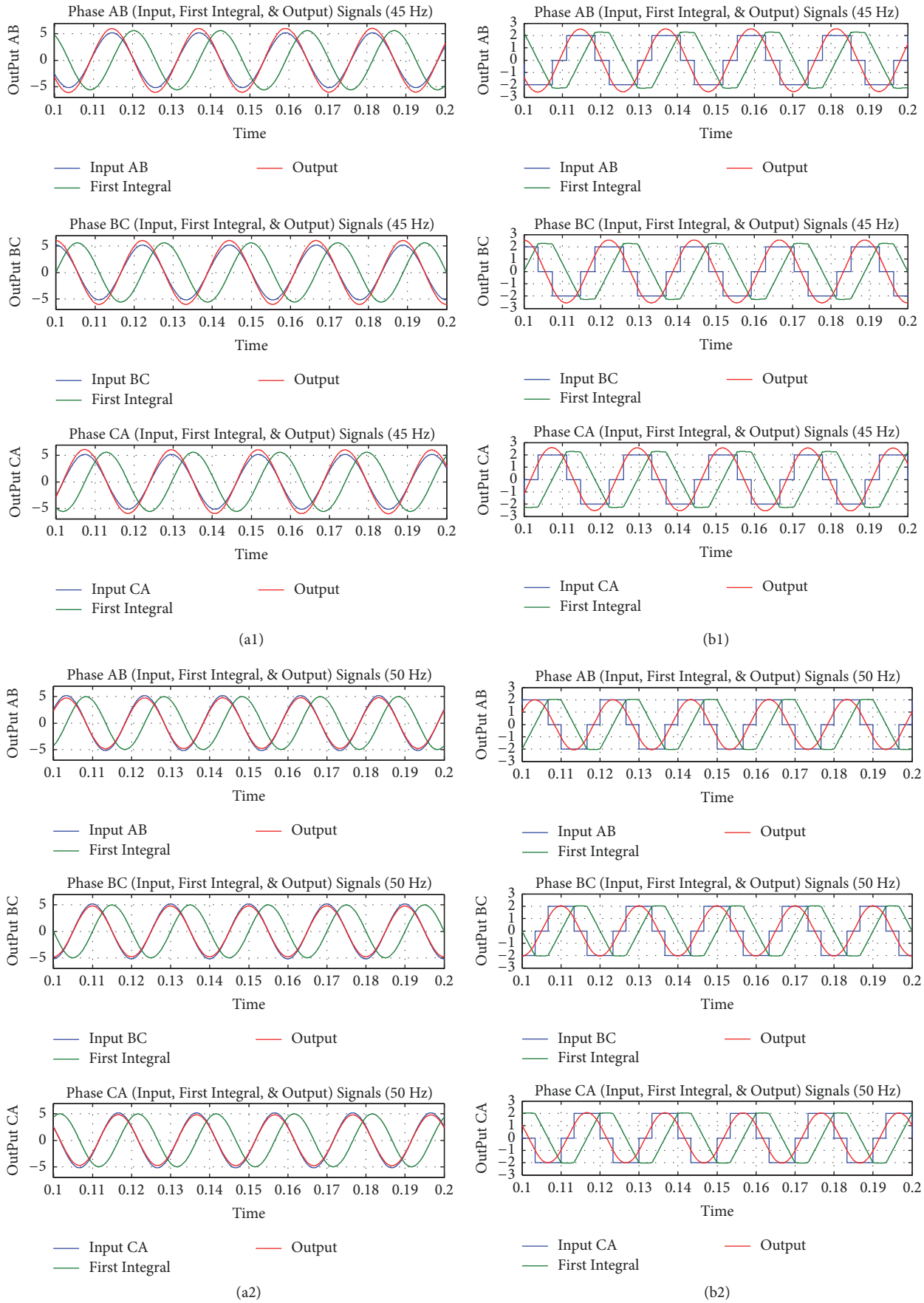


Figure 5: Continued.

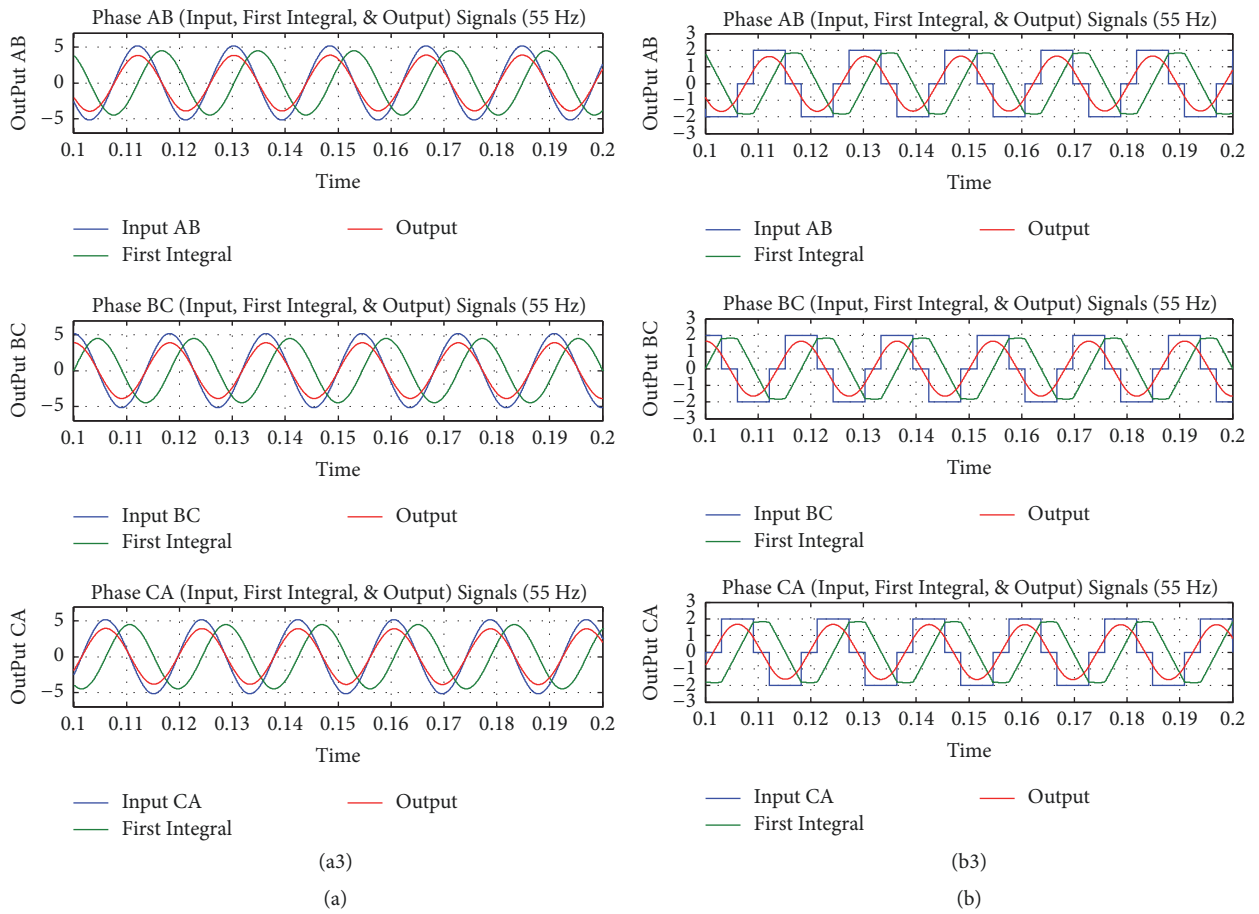


Figure 5: MATLAB/Simulink results of three-phase DISM (45, 50, and 55) Hz: (a) sine wave input signal; (b) square wave input signal.

## 5. Experimental Setup of SPWM for Three-Phase DISM

In order to verify the feasibility of the DISM of three-phase PWM, a DISM for digital circuit is shown in Figure 4, which was built in the laboratory as shown in Figure 7. This system shows the different power electronic blocks present on the full system of three-phase inverter. The main parts of the practical part can be classified as follows:

(i) dsPIC33FJ256GP710A with the Explorer 16 Development Board from microchip as a microcontroller.

(ii) Three-phase DC-AC inverter for photovoltaic application designed in the laboratory.

(iii) Three-phase LC filter and three-phase load.

(iv) DC power supply circuit.

(v) Three-phase voltage and current measuring circuits.

The dsPIC33FJ256GP710A microcontroller is used in this paper to control the full system of three-phase photovoltaic inverter. This type of controller is used for its high speed, especially in the applications of industrial applications that require accuracy and very high speed in control. This type has been used in industrial applications due to the low power consumption. Main pin terminals and the salient features are observed in Table 3 [11]. It is programmed by C language and using a MPLAB X IDEV3.65 software compiler for programing.

Figure 8 shows the experimental results waveform of digital circuit DISM. Figure 8(a) shows the SPWM results of upper and lower transistors of three-phase photovoltaic inverter depending to line-to-line voltage of grid. Figure 8(b) shows the results depending on phase to ground voltage of grid.

According to [26, 27], the voltage and current measurement circuit for the three-phase inverter was selected. Then, Figure 9 shows the comparison and sequence between three-phase grid voltage signals and output voltage signals of the inverter according to the DISM. These three-phase output signals will be injected from the photovoltaic inverter system into the grid after the relay has been verified with the grid signals.

## 6. Conclusions

This article has presented an alternative method to generate the reference signals of current for three-phase photovoltaic

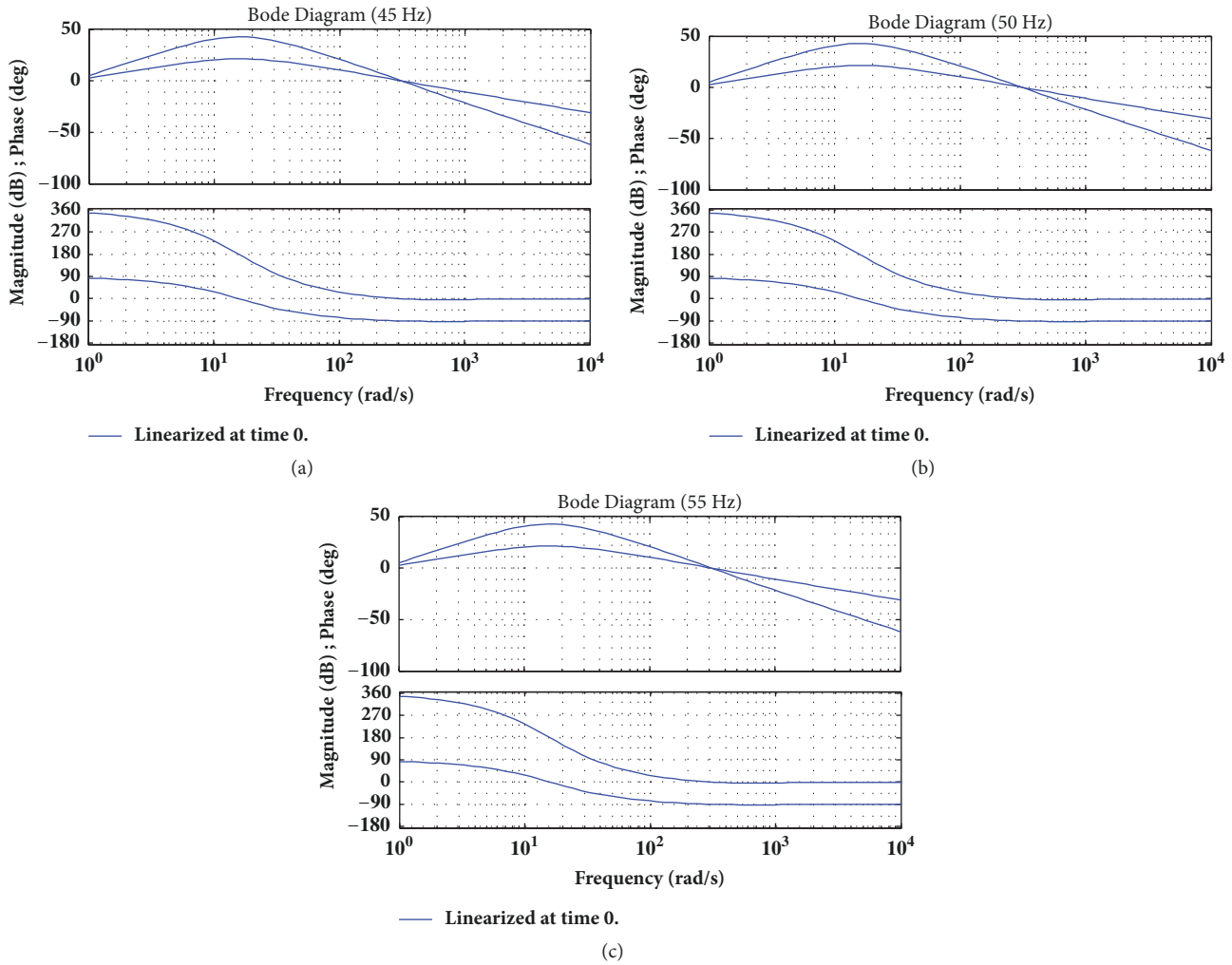


Figure 6: Bode plot diagram of single phase DISM: (a) 45Hz; (b) 50 Hz; (c) 55 Hz.

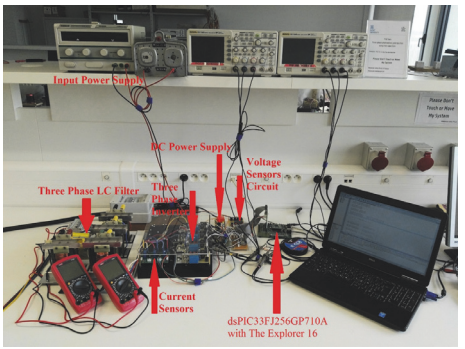


Figure 7: Three-phase hardware experimental setup of DISM.

Table 3: Specifications of dsPIC33FJ256GP710A.

| Device | Pins | Program Flash Memory (Kbyte) | RAM (Kbyte) | 16-bit Timer | Input Capture | Output Compare Std. PWM | ADC | UART | SPI | I/O Pins (Max) |
|---|---|---|---|---|---|---|---|---|---|---|
| dsPIC33FJ256GP710A | 100 | 256 | 30 | 9 | 8 | 8 | "2 ADC, 32 ch | 2 | 2 | 85 |


(a1-Phase A) (b1-Phase A)

(a2- Phase B) (b2- Phase B)

(a3- Phase C) (b3- Phase C)

(a) (b)

Figure 8: SPWM experimental results of digital circuit DISM: (a) three-phase SPWM (line-to-line voltage); (b) three-phase SPWM (phase voltage).

inverter. This method is called double integral synchronization method DISM. DISM is very important to synchronize the PWM for three-phase photovoltaic inverter depending on line-to-line voltage. Main advantage for this method in power electronics is to synchronize the grid voltage without needing any type of reference to compare the results. Analog and digital circuit were designed, implemented, and simulated by using MTLAB/Simulink. The Analog and Digital simulation circuits work successfully with good results. The final digital circuit was designed and implemented in the laboratory to generate the PWM depending on DISM to control the three-phase photovoltaic inverter. The dsPIC33FJ256GP710A with the Explorer 16 Development Board from microchip as a controller to generate the sinusoidal pulse width modulation was programed by C language and using a MPLAB X IDEV3.65 software compiler for programing.

The future of this work is to compare the double integral synchronization method with deferent type and techniques of phase looked loop (PLL) for single and three-phase grid–tide inverter application.

## Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

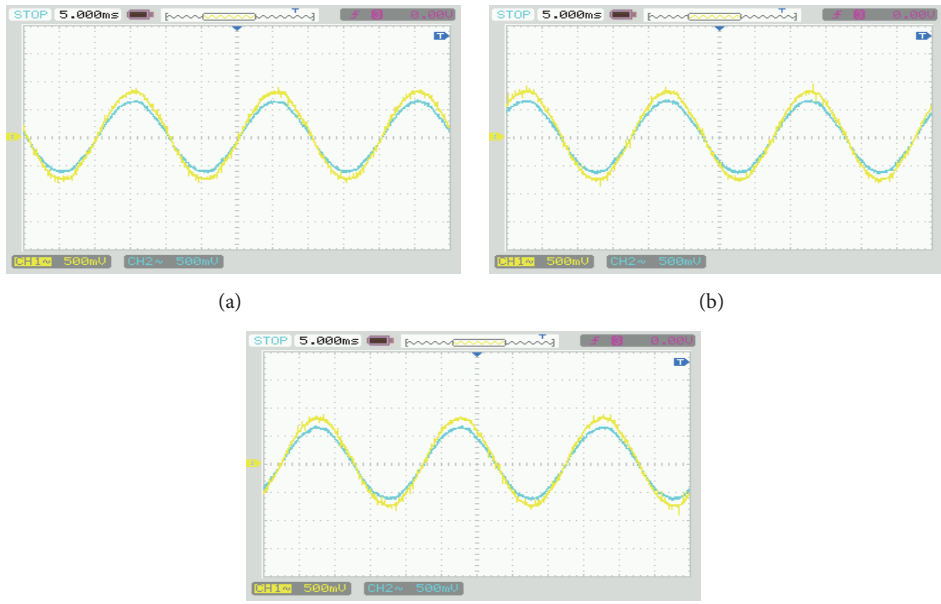


FIGURE 9: Grid voltage and output voltage of three-phase photovoltaic inverter with digital circuit of DISM. (a) Phase A; (b) phase B; (b) phase C. Note: Ch1 for inverter output voltage and Ch2 for grid voltage.

## Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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